**Experiment 7**

**M.S.SANJAY**

**15BCE0517**

**5(a). Full adder using 2 half adders**

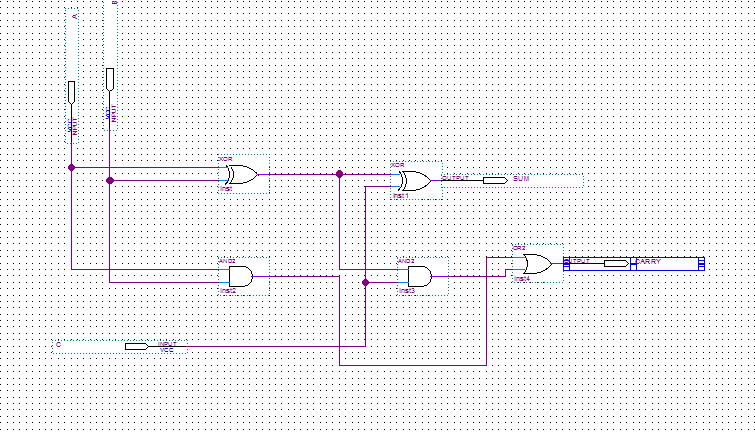
**Truth table:**

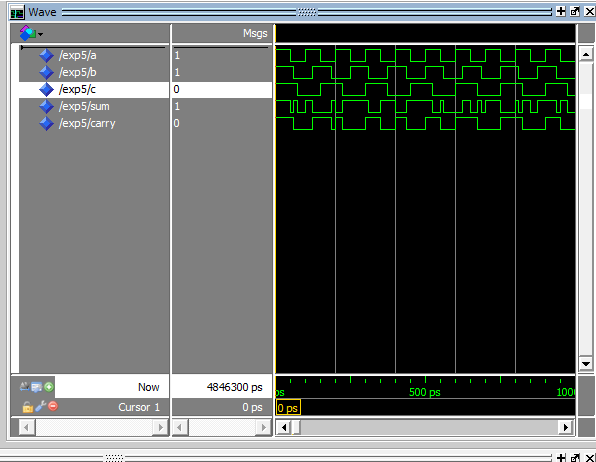
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **SUM** | **CARRY** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**Sum-**A xor B xor C

**Carry-**A.B + (A xor B).C

**Circuit layout:**



**Simulation waveform:**

**5(b).**Design a combinational circuit with three inputs, x, y, and z, and three outputs, A, B and C.

Using full adder and an inverter. When the binary input is 0, 1, 2, or 3, the binary output is one

greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than

the input

**Truth Table:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **X** | **Y** | **Z** | **A** | **B** | **C** |
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 |

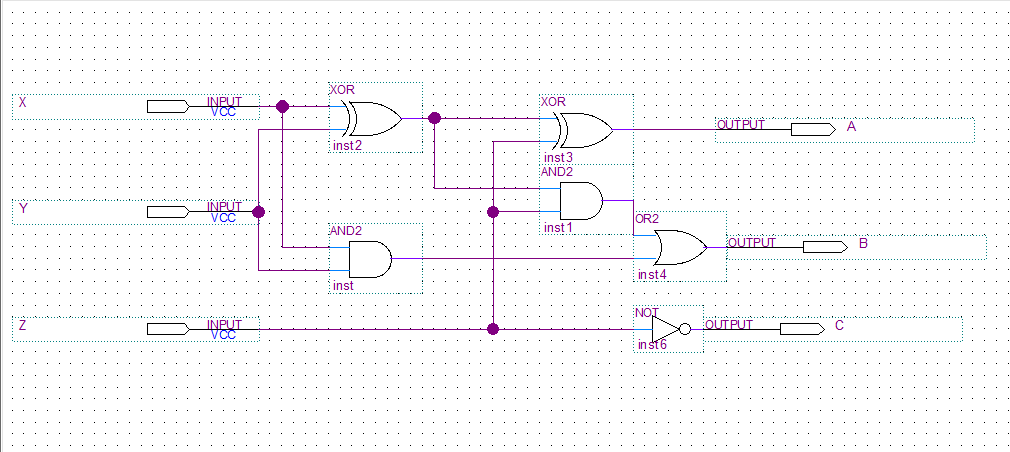
**Expression:**

**A=X.Y+X.Z+Y.Z**

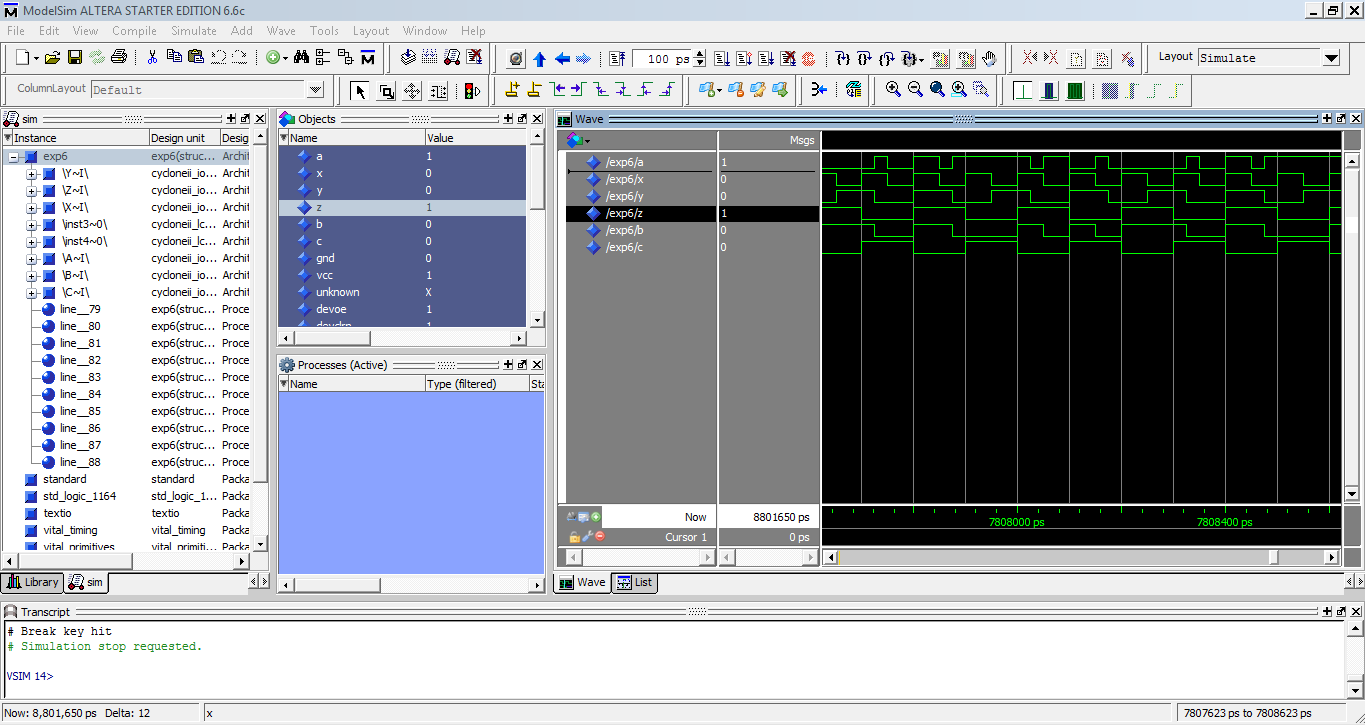
**B=X xor Y xor Z**

**C=Z’**

**Circuit layout:**

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**Simulation waveform:**

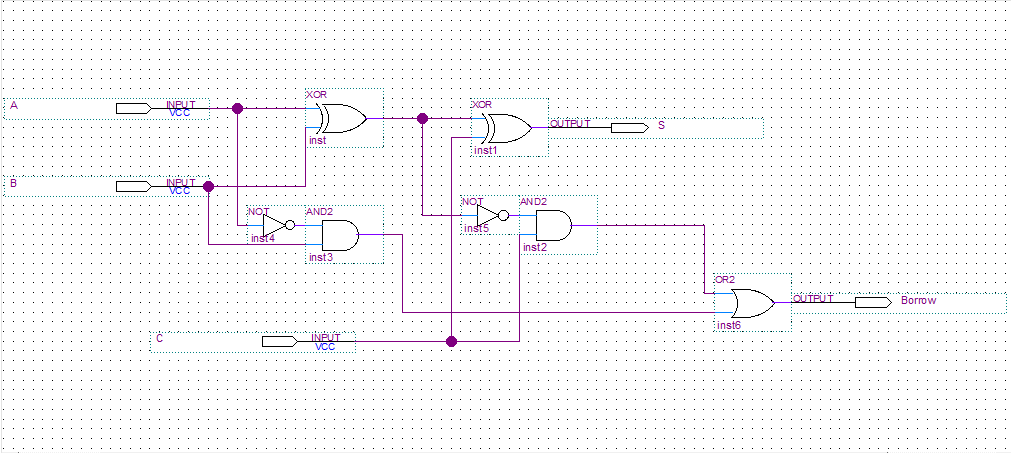
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**5(c). Design a full subtractor using two half subtractors.**

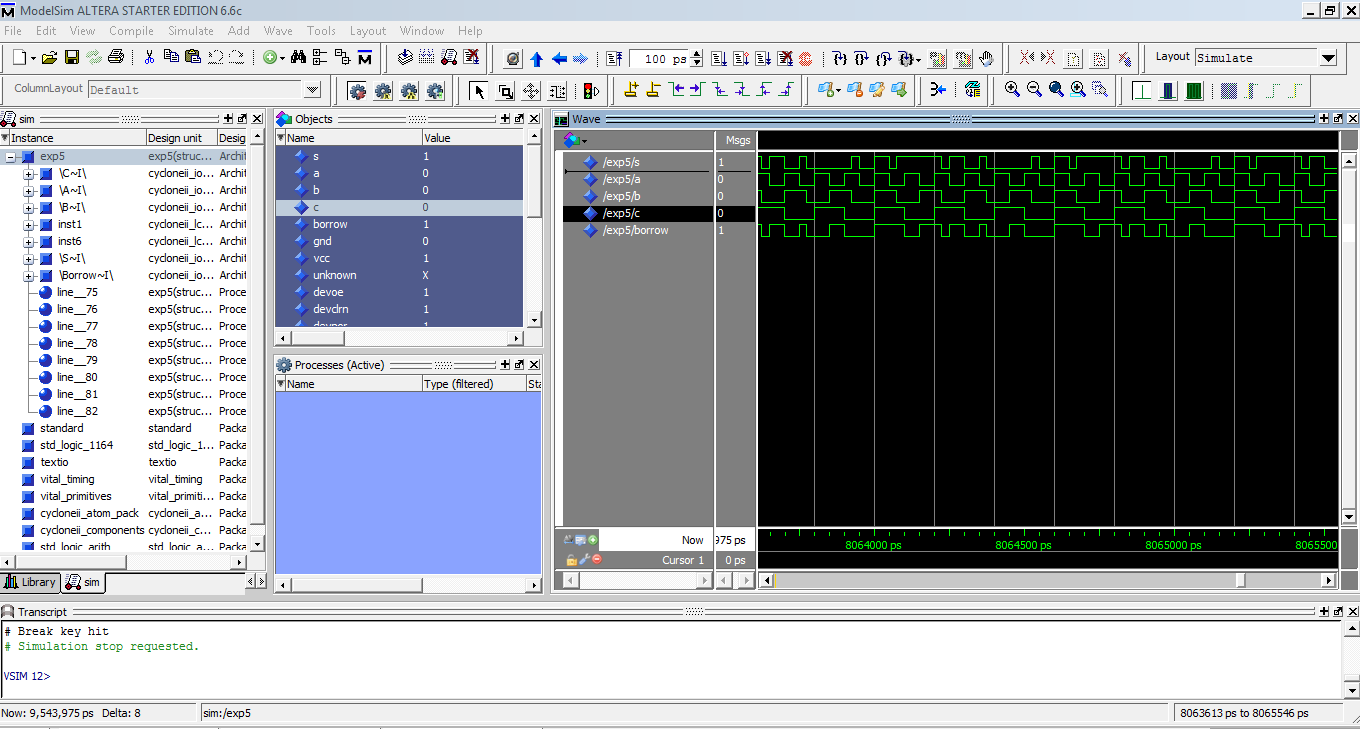
**Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **S** | **Borrow** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**Circuit layout:**

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**Simulation waveform:**

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**5(D).** Implement the four Boolean functions listed using three half -adders

D = A xor B xor C

E = A′BC + AB′C

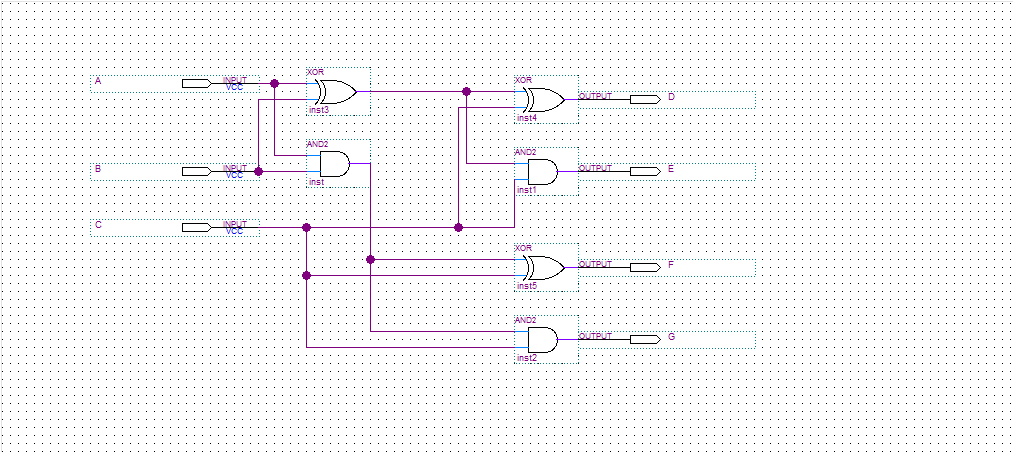
F = ABC′ + (A′ + B′)C

G = ABC

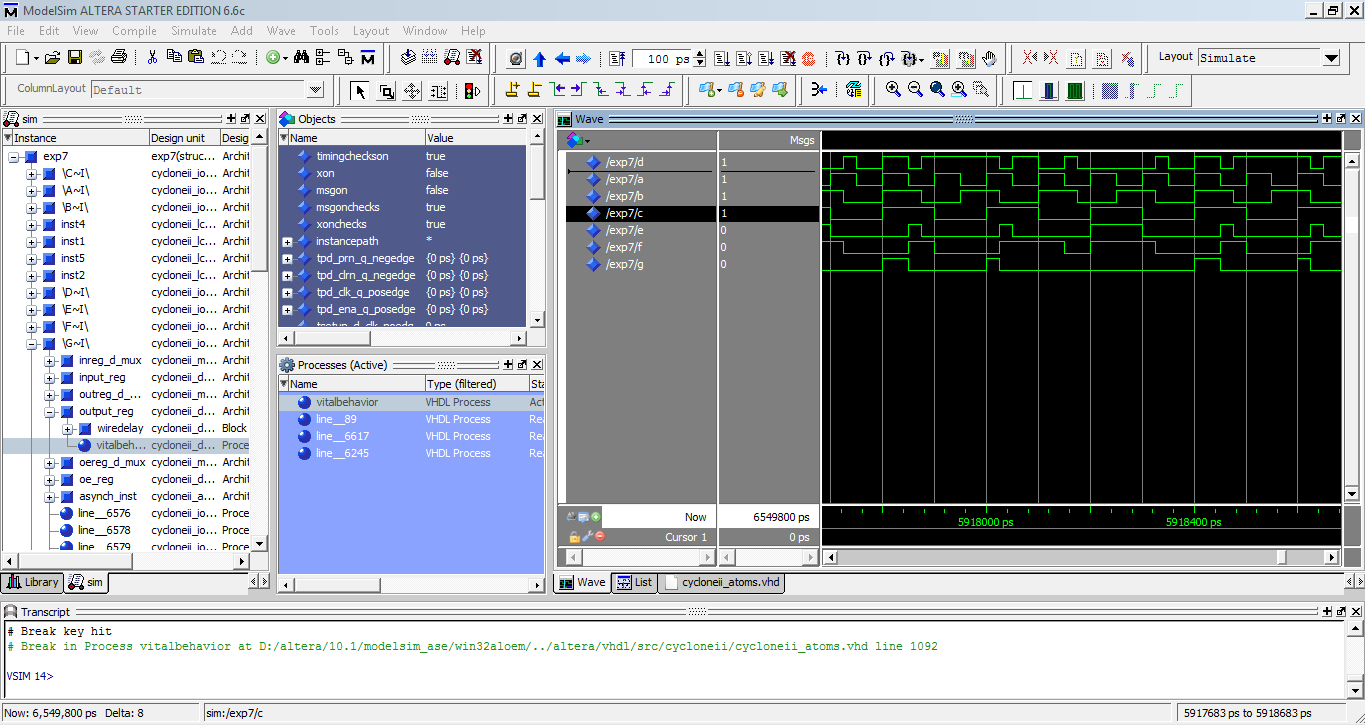
**Truth Table:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **E** | **F** | **G** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 |

**Circuit layout:**

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**Simulation waveform:**

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